A Compact Signal Generation and Acquisition Circuit for Electrochemical Impedance Spectroscopy

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Abstract—In this paper, a circuit for signal stimulus generation and response signal acquisition for electrochemical impedance spectroscopy (EIS) is presented. The circuit is capable of generating a stimulus signal consisting of 32 frequencies with a 2 Hz (low band) and a 62 Hz (medium band) step from 2 Hz to 2 kHz. A composite signal was generated from the circuit for one band at a time. Such composite signal provides a compact representation of the desired signal spectrum with 0.3% error. The response signal acquisition is accomplished with signal amplification followed by an ADC. An average error of 2.14% in measured impedance was achieved. The limit of detection of 9.2 Ohms was obtained. The design was implemented on a 2-layer PCB board with a total footprint of 75.26 cm^2.

Keywords—Electrochemical Impedance Spectroscopy (EIS); Point-of-Care (POC); Pathogen Detection

I. Introduction

As the quality of life improves markedly over the last several decades, interests in low-cost and highly mobile methods for disease prevention have grown significantly [1]. Early detection of virus and bacteria can help health care providers make decisions on effective treatments and prevent them from developing into serious diseases. Low-cost methods for pathogen detection in general are also highly desirable to make food and water safer. The traditional methods for pathogen detection, such as polymerase chain reaction (PCR) [2], offer high specificity with low limits of detection. Their disadvantages including the use of expensive thermocycler, specialized reagents, the need for fluorescent labeling, and laborious assay preparation steps [3] make them not suitable as a low-cost and high-mobile platform for pathogen detection. Electrochemical methods [4] provide alternatives to the traditional methods. One of the key advantages of electrochemical methods is that their transduction modes are based on measurement of changes in electrical property. This makes them highly suitable for low-cost and miniaturization. Electrochemical impedance spectroscopy (EIS) is a powerful method to analyze complex impedance changes. Results from EIS illustrate changes both in double layer capacitance and electron transfer resistance [5]. The spectrum curvature from EIS provides a signature for what an abnormal cell looks like, such as a tumor cell or tissue [6].

This paper presents a design for signal stimulus generation and response signal acquisition for EIS. The circuit is capable of generating a stimulus signal consisting of 32 frequencies with a resolution of 2 Hz at low frequency band and 62 Hz at medium frequency band. The frequency range for the stimulus signal is from 2 Hz to 2 kHz. This circuit generates
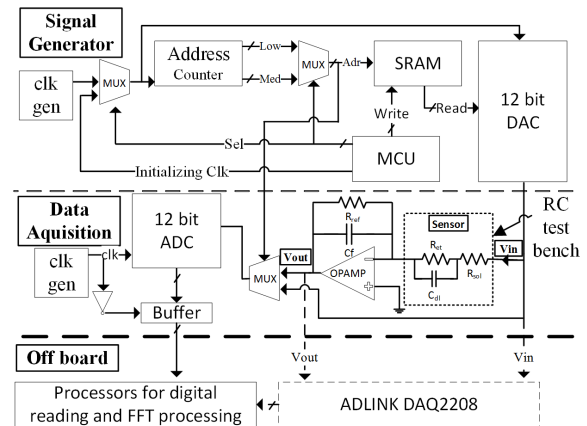

Fig. 1. System level architecture for proposed EIS device

a composite signal for one band at a time, which provides a compact representation of the desired signal spectrum with 0.3% error in amplitude among all frequency components. The response signal acquisition is accomplished with signal amplification using a transimpedance amplifier, followed by an ADC to generate digital outputs. An average error of 2.14% in measured impedance was achieved. The limit of detection 9.2 Ohms was obtained. The design was implemented on a 2-layer PCB board with a total footprint of 75.26 cm^2.

II. Existing designs

Manickam et. al. [7] proposed a method for measuring impedance using a lock-in amplifier. The backend circuit consists of a transimpedance amplifier (TIA), analog mixer and low pass filter (LPF). Their results showed that the output DC voltage is a strong function of sample's impedance. Similarly, Cassanos et. al. [8] proposed a lock-in amplifier based design with a higher level of integration to capture phase with adding a phase detection module. Their results showed good reproducibility and a measuring error of 1-4.5%. In [9], Ali et. al. showed a CMOS design based on charging period within a certain time interval as a function of sensor's impedance. Such an approach has the potential to improve SNR due to its simplicity and increased use of digital circuits. Maruyama et. al. [10] proposed an interdigitated array based implementation that provides spatial data from sample for imaging. Designs in [7]–[10] provided highly integrated approaches of measuring impedance changes for EIS. However, all these approaches

focused on response signal acquisition and did not attempt to address stimulus signal generation as part of their design. Stimulus signal generation for EIS generally requires a sweep of sinusoidal signals within a given frequency range. Effective stimulus signal generation for low cost and low power should be an integral part of the backend circuit. Yang et. al. [11] developed a signal generator that contains 31 sinusoidal signals using FPGA and DAC with good measured impedance results. The reported design in [11] only covered the signal generation. No response signal acquisition circuit was reported. [11] relied on a large signal magnitude to maintain sufcient signal-to-noise ratio (SNR) with the amplitude in the range of 250 mV for each harmonic and amplitude of the combined signal in the order of several volts. With applications using microelectrodes, higher the magnitude of stimulus signals, the more likely the potential damage to the electrodes, hence, the shorter the microelectrodes' lifetime and cause damage to the tissue or cell [12] [13]. A smaller signal amplitude is more desirable to optimize electrodes' lifetime. Furthermore, the work in [11] chosen a frequency band of 32 kHz to 992 kHz. For EIS, frequencies at sub-hundred Hz range is needed for detecting both electron transfer resistance and double layer capacitance [14]–[18].

III. PROPOSE SYSTEM LEVEL ARCHITECTURE

The EIS sensor circuit consists of stimulus signal generator, a measurement unit for impedance changes, and a response signal preparation and data processing unit. The system level design is shown in Fig. 1.

A. Stimulus Signal Generator

The stimulus signal generator combines 32 sinusoidal signals into a composite analog signal. To reduce the peak-to-peak magnitude of the combined signal, a low crest factor signal was designed by inserting phase offset to each individual sinusoidal signal frequency similar to that in [19].

A programmable microcontroller unit (MCU) is used to initialize the SRAM with digital samples of the composite signal. Each composite signal has 256 data points. The SRAM is driven by an address counter to select composite signal values in an incremental fashion. Multiplexers (MUX) controls the selection of two different frequency bands. The digital values of the composite signal are converted to their analog counterparts by a 12-bit DAC before being applied to sensor for impedance measurement. A clock generator synchronizes the composite signal generation process. The output from DAC acts as input signal to the sample.

B. Impedance Measurement Unit

The impedance measurement unit consists of a transimpedance amplifier (TIA) for converting the response current to an output voltage. The TIA uses an operational amplifier (opamp) with a reference resistor R_{ref} in the feedback. A capacitor, C_f, in parallel with R_{ref} is used for reducing TIA's output noise. The choice of R_{ref} and C_f is to prevent output railing within the estimated range of Z_{sensor} and TIA's

bandwidth and noise tradeoff requirement. In this design, a 1.91 kOhms resistor and 470 pF feedback capacitor were chosen.

C. Response Signal Preparation and Data Processing

The sensor response signal from the TIA is digitized by a 12-bit ADC. The digitized data can then be sent to host computer for further processing. The data processing consists of calculating magnitude and phase information about the sensor impedance using eqs. (1) and (2).

$$|Z_{sensor}| = \frac{R_{ref} \times \sqrt{V_{in,Real}^2 + V_{in,Imag}^2}}{\sqrt{V_{out,Real}^2 + V_{out,Imag}^2}} \quad (1)$$

$$\theta_{sensor} = \arctan \frac{V_{out,Imag}}{V_{out,Real}}$$

Overall, two steps are taken. 1). Select and sample V_{in} and V_{out} from the output mux and convert them the digital outputs. 2). Acquire digital outputs and run fast Fourier transform (FFT) processing, then calculate impedance for both magnitude and phase off-line. FFT is an algorithm that translates signal from time domain to frequency domain which fits to EIS application, it can also be realized directly through hardware for better integration level [20].

Low-power and compact FFT designs [20] also make it possible to integrate the FFT function into the sensor measurement unit.

IV. EXPERIMENTAL RESULTS

The input stimulus generation and output response acquisition circuits were implemented on a PCB using off-the-shelf components. Fig. 2 shows the PCB implementation of the proposed design. An equivalent RC test bench was built to mimic the electrode-electrolyte interface with a C_{dl}=15.6 uF, R_{et}=100 Ohms and R_{sol}=100 Ohms as shown in Fig. 1, where C_{dl} and R_{et} are the double layer capacitance and electron transfer resistance respectively at electrode-electrolyte interface, R_{sol} is the solution resistance.
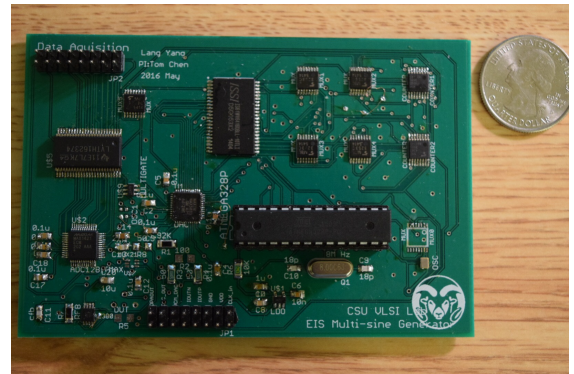

Fig. 2. PCB layout for proposed design

Fig. 3 shows the output from signal generator at output of DAC. The average amplitude for each frequency component is about 10.02 mV with a standard deviation of 28.65 uV. The signal spectrum is obtained using an ADLINK DAQ2208

data acquisition unit with an off-line FFT on a host computer. The output signal shows an excellent spectrum purity for the desired frequency range.
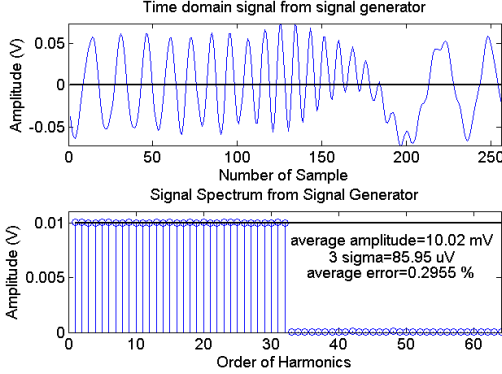

Fig. 3. Time & frequency domain composite signal from stimulus generator

The response from the RC test bench under the input stimulus from 2 Hz to 2 kHz was acquired with both off-board and on-board data acquisition (DAQ) methods. Fig. 4 shows the Bode plot of the response signal from the RC test bench using the off-board acquisition method and using HP4192A impedance analyzer.Comparing measurements using the signal generator and impedance measurement unit on the PCB and the output from using HP4192A, Fig. 5 shows impedance measurement error for each frequency in the desired range. The average impedance magnitude error is 0.86% while the phase error is 0.6 degree.
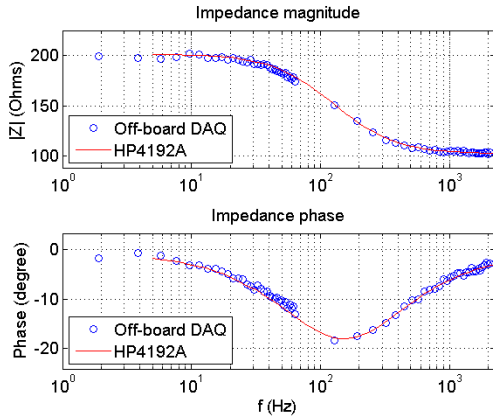

Fig. 4. Measured Bode plot from off-board data acquisition

Fig. 6 shows the noise spectrum density at output of TIA measured using the ADLINK data acquisition board. The intergraded input inferred noise of TIA is 1.58 uA, the limit of detection is when the input signal is equal to the noise. Eqs. (3) and (4) shows the relationships between the overall sensor impedance and the components in the equivalent circuit in Fig 1. Let V_{rms}=7.14 mV (10 mV amplitude), δI=1.58 uA, R_{et}=100 Ohms, R_{sol}=100 Ohms, C_{dl}=15.6 uF, the detection limit is 9.2 Ohms.
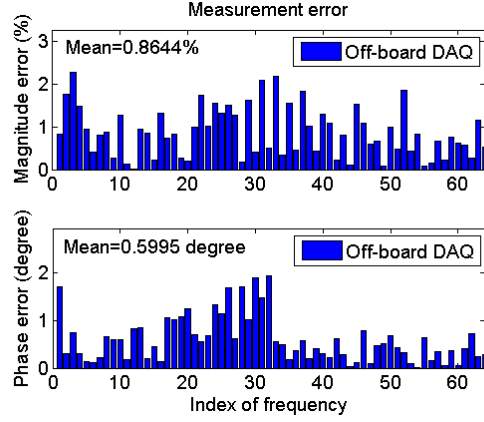

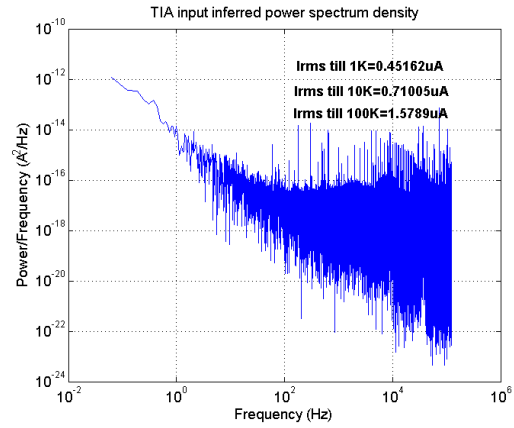Fig. 5. Measurement error from off-board data acquisition

Fig. 6. Input inferred noise spectrum density from TIA

Test with build-in ADC on the PCB board was also carried out. Fig. 7 shows the Bode plot similar to that in Fig. 4, but with the response signal from the built-in ADC output added. The average error for impedance magnitude and phase for the response from the built-in ADC output is 2.14% and is 1.58 degree respectively. The added error in both the impedance magnitude and phase can be attributed to the noise contribution from the built-in ADC. The corresponding Nyquist plot results from both off-board and on-board data acquisition methods are presented in Fig. 9.

$$\delta Z_{sensor} = \frac{\delta I \times |Z(\omega)|^2}{V_{RMS} - \delta I \times |Z(\omega)|} \qquad (3)$$

$$Z(\omega) = R_{sol} + \frac{R_{et}}{1 + \omega^2 R_{et}^2 C_{dl}^2} - \frac{j\omega R_{et}^2 C_{dl}}{1 + \omega^2 R_{et}^2 C_{dl}^2} \qquad (4)$$

V. Conclusions

A sensor circuit for EIS is presented in this paper. The circuit obtains the spectrum information using a multi-frequency composite signal without explicit sweeping of frequencies. The results are from the prototype board. The composite signal achieved 0.3% error in amplitude among all frequency
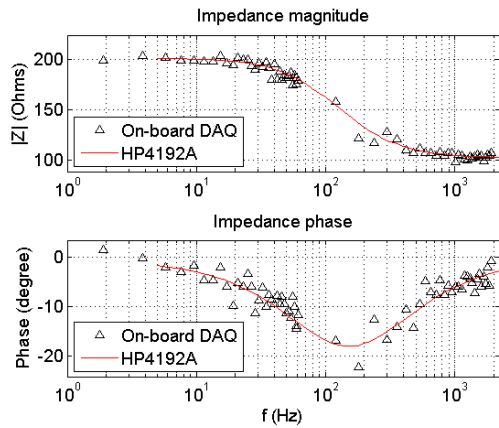
Fig. 7. Measured Bode plot from on-board data acquisition

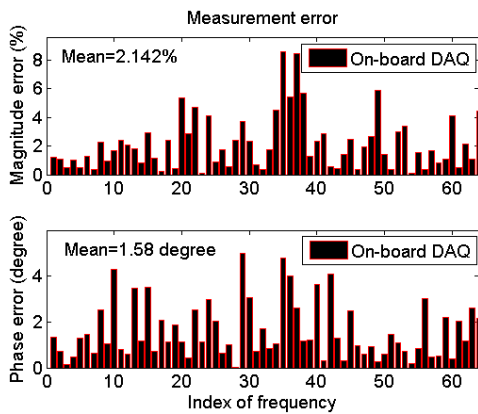Fig. 9. Nyquist plot from off/on-board acquisition approaches

Fig. 8. Measurement error from on-board data acquisition

components. An average error of measured impedance is 2.14%. The limit of detection of 9.2 Ohms makes the sensor suitable for practical applications. Potential improvements of the circuit include noise reduction and a wireless interface.

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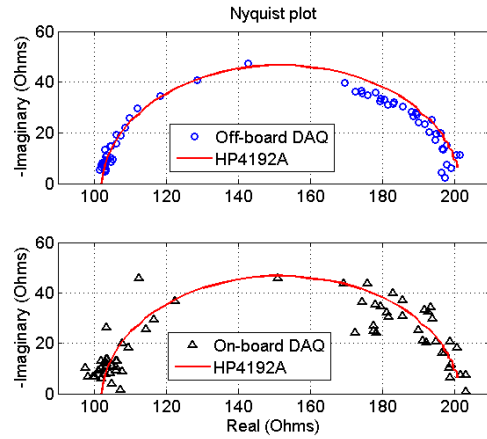
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